REMARKS

In response to the Office Action of April 16, 2007, please amend the claims as indicated.

Claim Objections

Claim 1 has been objected to for reciting "a bootstrap program executable by the processing unit" without reciting any structure (such as a bootstrap memory) for holding the bootstrap program. Applicant has amended claim 1 to positively recite a bootstrap memory. This bootstrap memory need not, but may be on the common integrated circuit substrate so long as it is communicating with the processing unit.

In claims 1 and 12 "selected set up data" has been amended as suggested by the Examiner to be --determined set up data--.

In claims 1, 3, 5 and 7-10 "external memory" has been changed to be --external random access memory--, as proposed by the Examiner. Claim 4 describes only "external memory setup data" and thus does not present the antecedent basis problem noted by the Examiner.

Claim 5 has been amended to indicate that the volatile memory and the nonvolatile memory are both external thus providing antecedent basis for these terms. Because the "external memory setup data" was for the "external random access memory" it follows that it may also be for the "external volatile memory" which is part of the "external random access memory".

Claim Rejections -- 35 U.S.C. §112

Claims 1-23 have been rejected under 35 U.S.C. §112 first paragraph because the specification does not disclose "a common integrated circuit substrate without general-purpose random access memory". Applicant respectfully disagrees. Paragraph [0006] notes that:

> An exception to this single "chip" integration is the memory system, such as random access memory (RAM) which, for reasons of flexibility, cost, and size may be implemented in one or more separate integrated circuits. Separating the RAM from the embedded processor allows greater flexibility in varying the amount of memory necessary for different embedded applications, allows for more efficient fabrication of the memory, and allows the designer to take advantage of rapidly changing advances in memory technology and design.

The application clearly indicates (for example at Fig. 2 and the related specification) that the random access memory (38) is not part of the embedded processor (12). The application is further clear that this is a feature that creates the problem to be solved by the invention.

The Applicant understands the Examiner's position to be based on an interpretation of "general-purpose random access memory" to include all memory structures associated with a processor including registers, caches, and buffers.

This interpretation is counter to the plain and ordinary meaning of the words "general-purpose random access memory" as would be understood in the art. Registers, caches, and buffers are special purpose memory structures that may not and frequently do not provide random access capabilities. The Examiner's interpretation is further counter to the express teaching of the present application which specifically distinguishes cache 24 or buffer 32 from general-purpose random access memory 38. Finally, the specification clearly requires that the "general-purpose random access memory" is not integrated with the embedded processor 12 but placed externally. To the Applicant's knowledge registers, caches, and buffers are never separated from the processing unit in an integrated processing system.

Claim Rejections -- 35 U.S.C. §102

Response to Arguments--paragraph 31

As noted above, the Applicant respectfully disagrees with the Examiner's assertion that the claim limitation of "a common integrated circuit substrate without general-purpose random access memory" is not taught in the specification. While the Examiner is free to give claims a broad interpretation, this interpretation must be both "reasonable" and "consistent with the specification". See MPEP §2111.

Accepting that the claims require an external, general-purpose random access memory, Fullam clearly teaches the opposite: a system where the "general-purpose random access memory" is integrated with the processing unit. Such on-board random access memory is common in smaller processors and is implicit in Fullam because random access memory is required for any computer operation and no external random access memory is shown or described. There is no support in the sections cited by the Examiner (column 1 lines 31-32; column 6, lines 59) for the proposition that Fullam executes programs using cache memory in lieu of general-purpose random access memory.

Response to Arguments--paragraph 32

The Examiner is inconsistent in the interpretation of memory 58 in Fullam. The Examiner identifies memory 58 of Fullam as an external random access memory, relying on

column 1, lines 33-34 in order to meet the claim limitations of claim 1 requiring an external random access memory. See pages 4, lines 3-5 of the present office action. But the Examiner also asserts that Fullam does not have write access to memory 58, apparently because memory 58 is not a random access memory but a read-only memory. See page 10, paragraph 31 of the present office action. This is in order to meet the claim limitation in claim 1 that the bootstrap program be executed without write access.

A consistent interpretation of Fullam, is that Fullam teaches that from the instant of power up, the processor may communicate with the external memory. See column 7, lines 27-31. This access would clearly include write access, if memory 58 were a random access memory as indicated by the Examiner because the same knowledge that allows read access allows write access. In this case Fullam fails to teach element (i) of claim 1. Alternatively this access may include only read access, if memory 58 is a read only memory and must always be a read-only memory, but then Fullam fails to teach element (ii) of claim 1.

Response to Arguments--paragraph 33

The Applicant respectfully disagrees that Fullam teaches a network interface as claimed in claims 4 and 15. The Examiner has provided no support for this assertion except to state that claims 4 and 15 do not require a "sophisticated network protocol" by their terms. The Applicant does not need to rely on claiming a "sophisticated network protocol" because Fullam does not teach a network interface as claimed.

Fullam teaches away from the innovation of the present invention by describing a system that has an on-board general-purpose random access memory. Fullam does not explicitly describes this onboard general-purpose random access memory, but it is implicit and would be understood to those of ordinary skill in the art based on the fact that this structure is common whereas the structure of no random access memory can be found only in the present application. The lack of description in Fullam would not lead one of ordinary skill in the art to believe that Fullam had developed a novel method of executing programs without access to a general-purpose random access memory. Fullam does not provide sufficient description of how a program could be executed without access to a general purpose random access memory in ordered to be enabling and thus cannot anticipate the present invention.

Because Fullam teaches that access to an external memory can be had in a special "slow mode" a person of ordinary skill in the art reading Fullam and wanting to eliminate an on-board general-purpose random access memory would simply use an off-board general-purpose random access memory accessed in the slow mode during the bootstrap process.

In light of these amendments and comments it is believed that rejection of the claims is overcome and allowance of claims 1-23 is respectfully requested.

Respectfully submitted,

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